REMARKS

Attached is a marked-up version of the changes being made by the current amendment.

Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: (b/1/0)

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Version with markings to show changes made

In the specification:

Figure<u>s</u> 3 <u>and 4</u> is a schematic block diagram of accelerated graphics port (AGP) functionality of a graphics memory controller hub.

Referring to Figure<u>s</u> 3 <u>and 4</u>, AGP transactions are run in a split transaction fashion in which a request for data transfer to or from system memory 4 is disconnected in time from the data transfer itself. An AGP compliant graphics device (bus master) 7a initiates a transaction with an access request. The AGP interface 21 responds to the request by directing the corresponding data transfer at a later time, which permits the AGP graphics device 7a to pipeline several access requests while waiting for data transfers to occur. As a result of pipelining, several read and/or write access requests may be simultaneously outstanding in request queues 100. Access requests can either be pipelined across an address/data bus (AD bus) 105, 107 of AGP 9 or transferred through sideband address lines 107 of AGP 9 and received by request queue 100.